TWO LEVEL LOGIC MINIMIZATION CAD TOOL FOR SINGLE OUTPUT BOOLEAN FUNCTIONS

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Integration density and performance of integrated circuits have gone through an astounding revolution in the last couple of decades with the evolution of computer. Minimization of Boolean functions plays a prime importance in gaining the integrating density and specially the performance in reducing the propagation delay.

Various methods of minimization techniques such as Karnaugh Map method, Quine McCluskey method etc, have been introduced, but with the increasing number of input variables, these conventional methods become too complex and tedious. For example, when using the Karnaugh Map method more than with six input variables, it is too complex to minimize the function and even it is error prone.

In this paper, an efficient CAD tool for minimizing a Boolean function with any number of input variables has been proposed. This tool is capable of providing the best solution to a given Boolean Function. The inefficiencies of data structures used in the existing methods have also been addressed in developing this CAD tool.